REMARKS

After entry of this amendment, claims 1, 3, 10-24 and will be pending in this application. Claims 1 and 10 have been amended. Claims 21-24 have been added. Support for the new and amended claims can be found in the specification. No new matter has been added.

Claims 1, 3, and 10-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Deering et al., United States patent number 5,745,125. Reconsideration of this rejection and allowance of all the pending claims in light of the amendments and remarks is respectfully requested.

Claim 1

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Deering et al. But Deering et al. do not show or suggest each and every element of claim 1. For example, claim 1 as amended recites "a first shared operand unit...for simultaneously providing a first shared operand to the first MAC unit for computing a first result...and to the second MAC unit for computing a second result." The apparatus shown in Deering et al. is configured such that it cannot provide this feature.

The pending office action identifies the SRAM 153 in Figure 6 as being the shared operand unit. (See office action mailed June 24, 2002.) But the SRAM cannot provide a shared operand to a first MAC unit and a second MAC unit simultaneously as required by the claim.

Rather, the first MAC unit cited by the office action resides in the F-core 352 while the second is in the S-core 356 in Figure 6 of Deering. The SRAM 153 is separated from the S-core by the FS Buffer 384. Accordingly, the SRAM 153 cannot provide an operand simultaneously to a first and second MAC unit as required. For at least this reason, claim 1 should be allowed.

Other Claims

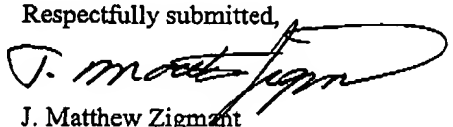
Claim 10 should be allowed for at least similar reasons as claim 1, and for the additional limitations it recites.

Claims 3 and 11-20 depend on claims 1 and 10 and should be allowed for at least similar reasons as claims 1 and 10, and for the additional limitation they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance and an action to that end is urged. If the Examiner believes a telephone conference would aid in the prosecution of this case in any way, please call the undersigned at 650-326-2400.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) An integrated circuit for image frame rendering and DSP applications, the integrated circuit during operation operating with memory, the integrated circuit comprising:

an interface circuit configured to control access to said memory, the interface circuit coupled to said memory;

an embedded processor configured to control the integrated circuit, the embedded processor configured to control the interface circuit to receive information therefrom; and

an array processor for performing arithmetic calculations, the array processor coupled to the interface circuit to receive information therefrom and connected to the embedded processor via an internal bus;

wherein the array processor comprises:

a first multiply/accumulator (MAC) unit coupled to a first local memory, the first local memory comprising a first plurality of operands;

a second MAC unit coupled to a second local memory, the second local memory comprising a second plurality of operands; and

a first shared operand unit coupled to the first MAC unit and the second MAC unit for simultaneously providing a first shared operand to the first MAC unit for computing a first result in association with the first plurality of operands and to the second MAC unit for computing a second result in association with the second plurality of operands; and

wherein the first result and the second result are computed independently of each other; and

wherein the array processor further comprises:

a second shared operand unit coupled to a third MAC unit and a fourth MAC unit for providing a second shared operand to the third MAC unit and the fourth MAC unit.

10. (Amended) An integrated circuit using a memory, said integrated circuit comprising:

an interface circuit configured to control access to said memory, said interface circuit coupled to said memory;

an embedded processor configured to control said integrated circuit, said embedded processor receiving information from said interface circuit; and

an array processor for performing mathematical calculations on data received from said interface circuit and connected to said embedded processor via an internal bus, said array processor comprising:

a plurality of multiplier/accumulator circuits; and

a plurality of shared operand circuits coupled to said plurality of multiplier/accumulator circuits for simultaneously providing a shared operand to at least two of said plurality of multiplier/accumulator circuits.